## CLAIMS

What is claimed is:

1. A *sample-and-hold peak detector circuitry comprising*
   - a comparator circuit comprising two signal inputs and a signal output where the output signal depends on the difference between the input signals,
   - a sample and hold circuit comprising switching means controlled by said signal output for sampling and holding means for holding the output signal,
   - a compensation circuit for compensating residual currents comprising emulating means for emulating residual currents caused by said comparator circuit influencing the functionality of said sample and hold circuit, and
   - an unload circuit comprising a clearing means for decreasing the output signal of said sample and hold circuit,

   wherein said compensation circuit comprises copies of parts of the comparator circuit as emulating means.

2. The circuitry according to claim 1 wherein said compensation circuit comprises a current mirror circuit mirroring residual currents emulated by said emulating means.

3. The circuitry according to claim 1 wherein said unload circuit comprises a constant current source.

4. The circuitry according to claim 3 wherein said constant current source is an adjustable constant current source.

5. The circuitry according to claim 4 wherein said adjustable constant current source is realized by multiple switchable constant current sources.

6. The circuitry according to claim 5 wherein said switchable constant current sources are switchable by transfer gates.

7. The circuitry according to claim 1 wherein said comparator circuit is implemented in differential logic.

8. The circuitry according to claim 1 wherein said comparator circuit comprises a current switch and a constant current source.

9. The circuitry according to claim 7 wherein said differential logic is a differential emitter coupled logic.